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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,226	10/24/2003	Zohar Bogin	42P17980	2284

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Chui-Kiu Teresa Wong
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
WEINMAN, SEAN M	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,226	BOGIN ET AL.	
	Examiner	Art Unit	
	Sean Weinman	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 October 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/24/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-28 are presented for examination.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Reference character 402 in Figure 4 is not mentioned in the description. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Attaway et al. (US Patent No. 6,829,677) in view of Applicant's Admission of Prior Art (AAPA)

As per claim 1, Attaway et al. teaches the claimed invention comprising:

causing a reset of the system if the plurality of memory devices are not initialized *(Col. 8 lines 1-7)*; and

enabling a deterministic shutdown mode in a memory controller coupled to the plurality of memory devices after the plurality of memory devices have been initialized *(Col. 7 lines 65-67 and Col. 8 lines 1 and 7-31).*

Attaway et al., however, does not teach that causing a first type of reset in a plurality of memory devices in a system in response to a second type of reset being initiated, different than the first type of reset, in the system. Specifically, Attaway et al. teach detecting whether or not a memory system is initialized or not being initialized. Additionally, Attaway et al. teach putting the memory controller in a deterministic shutdown mode if the memory system is initialized or resetting the system if the memory system is not being initialized. Attaway et al. does not teach that causing a first type of reset to a system in response to a second type of reset in the system.

The AAPA teaches the causing a cold reset in a plurality of memory devices in a system in response to a warm reset. AAPA teach causing a first type of reset in a plurality of memory devices in a system in response to a second type of reset being initiated, different than the first type of reset, in the system

(Paragraphs [0003] - [0006]). In summary, the AAPA teaches causing a cold reset in the system response to a warm reset being initiated.

It would have been obvious to combine the teaching of Attaway et al. and the AAPA because they both teach systems for resetting memory controller in response to a user initiated reset. AAPA teaches the deficiency of Attaway et al. by teaching that the causing a first type of reset in a plurality of memory devices in a system in response to a second type of reset being initiated in the system.

As per claim 2, Attaway et al. teach the claimed invention comprising:

putting the plurality of memory devices into a known state in response to the second type of reset being initiated in the system if the deterministic shutdown mode is enabled *(Col. 7 lines 65-67 and Col. 8 lines 1 and 7-31)*.

As per claim 5, Attaway et al. teach the claimed invention comprising:

wherein the known state is a self-refresh state *(Col. 7 lines 65-67 and Col. 8 lines 1 and 7-31)*.

As per claim 6, Attaway et al. teach the claimed invention comprising:

wherein the plurality of memory devices comprises one or more double data rate synchronous dynamic random access memory devices *(Attaway et al. teaches the memory devices being SDRAM. It would have been obvious to one of ordinary skill in the art for one the memory devices to be DDR SDRAM)*.

As per claim 7, the AAPA teaches the claimed invention comprising:

wherein the first type of reset is a cold reset and the second type of reset is a warm reset *(Paragraphs [0003] - [0006])*.

Claims 3, 4, and 8-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Attaway et al. (US Patent No. 6,829,677) and Applicant's Admission of Prior Art (AAPA) as applied to claims 1, 2, and 5-7 above, and further in view of George (US Patent No. 6,119,200).

As per claims 8 and 17, Attaway et al. and the AAPA teach the claimed invention for all of the reasons stated above. Additionally, Attaway et al. teach a switch to enable the deterministic shutdown mode when the pluralities of SDRAMs have been initialized *(Col. 7 lines 65-67 and Col. 8 lines 1 and 7-31 Attaway et al. does not explicitly teach as switch to enable the deterministic shutdown mode but it obvious that a switch must exist for the memory controller to respond in the proper mode to the reset signal)*. Additionally, the AAPA teaches a plurality of SDRAMs and a memory controller, coupled to the plurality of SDRAMS *(Paragraphs [0003] - [0006])*. Specifically, Attaway et al. and the AAPA teach a memory controller, having a plurality of memory devices, that operates in deterministic shutdown mode when the devices are being initialized and resets when the devices are not being initialized. Attaway et al. and the AAPA, however, do not teach a detector to detect a reset signal and a gate to hold the reset signal if the memory controller is in deterministic shutdown mode and reset the memory controller if the deterministic shutdown mode is disabled.

George teaches another system for resetting memory controller of SDRAMs in response to a user initiated reset. George teaches the claimed invention comprising:

a detector to detect a reset signal *(Col. 5 lines 19-28 George does not explicitly teach a detector but it would be obvious to one of ordinary skill in the art that a detector be present to detect a warm reset event)*; and

a gate to gate the reset signal if the deterministic shutdown mode is enabled and to pass the reset signal to a logic unit if the deterministic shutdown mode is not enabled *(Col. 5 lines 19-28 George does not explicitly teach a gate to gate the reset signal but it would obvious to one of ordinary skill in the art that a gate would be present to block and release the reset signal)*. In summary, George teaches a detector to detect when the memory controller has received a reset and additionally to block and receive that reset based on the operation of the memory controller at the present time.

It would have been obvious to combine the teachings of Attaway et al., AAPA, and George because they all teach systems for resetting memory controller for SDRAM in response to a user initiated reset. George teaches the deficiency of Attaway et al. and the AAPA by teaching a detector to detect the reset signal and a gate to hold and pass the reset signal based on the operation of the memory controller.

As per claim 3, 14, and 23, the Attaway et al. teaches the claimed invention comprising:

resetting in a plurality of stages a plurality of logic blocks in the memory controller while putting the plurality of memory devices into the known state *(Col. 7 lines 65-67 and Col. 8 lines 1 and 7-31 Attaway et al. teaches resetting the rest of the system while the memory devices are being put in a known state)*.

As per claim 4, the George teaches the claimed invention comprising:

comprising resetting the memory controller after the plurality of memory devices have been put into the known state *(Col. 5 lines 19-28).*

As per claims 9 and 18, the Attaway et al. teach the claimed invention comprising:

a sequencer, coupled to the detector, to cause the logic unit to put the plurality of memory devices into a known state in response to the second type of reset being initiated if the deterministic shutdown mode is enabled *(Col. 7 lines 65-67 and Col. 8 lines 1 and 7-31 Attaway et al. does not explicitly teach a sequencer to cause the logic to put the devices into a know state but it would obvious to one of ordinary skill that a sequencer must be present for the memory controller to put the memory devices into a known state).*

As per claims 10 and 19, the George teaches the claimed invention comprising:

the sequencer causes the gate to pass the reset signal after the plurality of memory devices have been put into the known state *(Col. 5 lines 19-28).*

As per claims 11, 12, 20, and 21, the Attaway et al. teach the claimed invention comprising:

sequencer receives one or more signals from the memory cycle tracker and command generator to determine whether the plurality of memory devices have been put into the known state *(Col. 7 lines 65-67 and Col. 8 lines 1 and 7-31 Attaway et al. does not explicitly teach a command generator or a memory cycle tracker but it obvious to one of ordinary skill in the art that these must exist*

for the memory controller to know the state of the memory devices and also to put the memory devices into a known state).

As per claims 13 and 22, Attaway et al. teach the claimed invention comprising:

wherein the known state is a self-refresh state *(Col. 7 lines 65-67 and Col. 8 lines 1 and 7-31).*

As per claims 15 and 24, Attaway et al. teach the claimed invention comprising:

wherein the plurality of memory devices comprises one or more double data rate synchronous dynamic random access memory devices *(Attaway et al. teaches the memory devices being SDRAM. It would have been obvious to one of ordinary skill in the art for one the memory devices to be DDR SDRAM).*

As per claims 16 and 25, the AAPA teaches the claimed invention comprising:

wherein the first type of reset is a cold reset and the second type of reset is a warm reset *(Paragraphs [0003] - [0006]).*

As per claim 26, the Attaway et al. teaches the claimed invention comprising:

a processor coupled to the memory controller *(Figure 1 Reference character 102).*

As per claim 27, the Attaway et al. teaches the claimed invention comprising:

processor initiates the second type of reset in response to a user request or a software application *(Col. 7 lines 53-64)*.

As per claim 28, the AAPA et al. teaches the claimed invention comprising:

an input/output controller, coupled to the memory controller, to store a bit to indicate whether the plurality of SDRAMs are initialized (*AAPA does not explicitly teach a I/O controller but it is inherent that one must exist to for the memory controller to detect whether the memory devices are initialized)* .

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sean Weinman
Examiner
Art Unit 2115